A NOVEL MMIC, X-BAND, PHASE SHIFTER

K Wilson, J M C Nicholas and G McDermott

GEC Research Laboratories, Hirst Research Centre, Wembley, England

ABSTRACT

A novel, single chip, monolithic, four bit phase shifter is described.

The first sample to be measured exhibited full 360° coverage at the design frequency, operation throughout X band, good match and an insertion loss of 5-8 dB.

INTRODUCTION

Most of the MMIC phase shifters reported to date have suffered from large chip area(s) or high insertion loss or demanding processing and sometimes all three.

Reported here is a complete 4-bit, MMIC, X-band phase shifter on a single chip only 3.7 x 2.3 mm. This chip gives 16 states at nominally 22.5 degree increments, has an insertion loss of ~5 dB and is fabricated with a relatively undemanding 2 μm technology.

The circuit configuration is believed to be entirely novel and is eminently suitable for MMIC construction since it consists of a number of identical sections. It is not, however, suitable for a discrete component or hybrid implementation as the component and assembly costs would be high.

THE CIRCUIT CONFIGURATION

This is shown in Figure 1. It consists of a 90° coupler of which ports 1 and 2 are the r.f. input and output and ports 3 and 4 are each connected to a transmission line along which are tapped a number of shunt switches to ground.

All switches are normally open except for one pair. An input signal applied to port 1 of the coupler will split equally between the two tapped transmission lines, be reflected from the closed switch pair, recombine in the coupler and appear at the output, port 2. The total phase shift is controlled by the choice of which switch pair to close. Loads are provided on the remote ends of each line to absorb any leakage past the switches.

Note that this circuit gives a time delay and not a 'phase shift' control. This is, in fact, the preferred characteristic for phased array applications.

DESIGN CONSIDERATIONS

To preserve a good (internal) match at all frequencies and phase states it is necessary that the tapped lines be of 50 ohms impedance. Furthermore, since this is a reflection circuit, the transmission phase shift between successive switches should be half the phase increments required from the circuit. The usual expressions:

$$Z_0 = \sqrt{L/C} \qquad \phi = \omega \sqrt{L.C}$$

can be used to calculate the required inductance and capacitance per section for a prototype design. For a 4-bit (16 x 22.5°) circuit the values required are:

$$L = 156 \text{ pH} \qquad C = 0.06 \text{ pF}$$

Since this low capacitance will be provided mainly by the stray capacitance of the switches the structure is designed as an artificial line consisting of a series of low pass sections. This also results in a useful size reduction so minimising chip area.

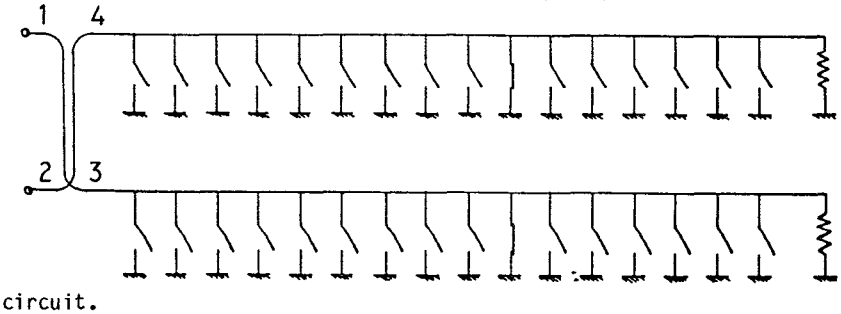

Figure 1 : The basic circuit.

Now consider the switching elements. These should have an on state resistance very much lower than 50 ohms, say 5 ohms, to get a low loss reflection from the closed switch pair and must also have an off-state capacitance which is no greater than the 0.06 pF calculated above. FET switches exceed this maximum CR product by a very large margin. Schottky diodes have therefore been chosen as the switching elements; these can meet the CR requirement although the power handling capability has to be considered.

Power handling is limited by the reverse breakdown voltage and by the forward current carrying capability of the diodes; the latter is set by electromigration in the diode contacts. Detailed calculation is too trivial to be reproduced here. The diode design employed for this circuit has a breakdown voltage of 6 volts and a current capability of 50 mA giving a power handling capability for the complete circuit of 30 mW. Receiver local oscillators and transmitter drivers can thus both be comfortably controlled by this chip.

Insertion loss is calculated to be ~5 dB. The two main contributions being ~2 dB from the diode 5 ohm on-resistance and ~1.5 dB from the two passes through the 0.75 dB loss of the coupler. These contributions are independent of the state of the circuit. Other minor contributions which are state dependent result from the inductor resistance and the diode off-state conductance.

The final design consideration is bandwidth. The main limitation here is the near octave bandwidth of the coupler although it must be remembered that a linear phase/frequency characteristic will be obtained in band.

LAYOUT

A complete chip is shown in Figure 2. An unfolded Lange coupler is used to enable r.f. input and output ports to be located on opposite short sides of the chip and the switching diodes are arrayed along the two long sides. Easy access for control signals is thus provided.

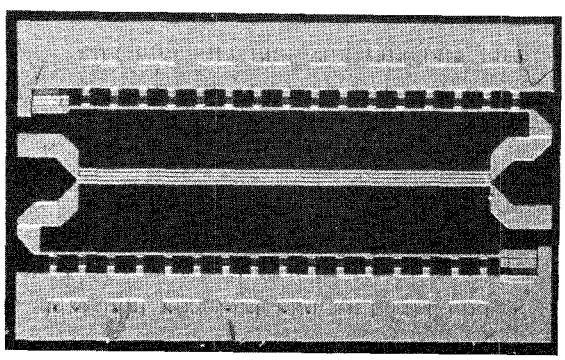

Figure 2 : The 4/bit phase shifter chip.

The control signals are applied across decoupling capacitors located in series with the earthy ends of the diodes and return via the dummy loads terminating the remote ends of the lines.

The inductors in each section are provided by the straight narrow tracks joining the 'hot' ends of the diodes; see detail in Figure 3.

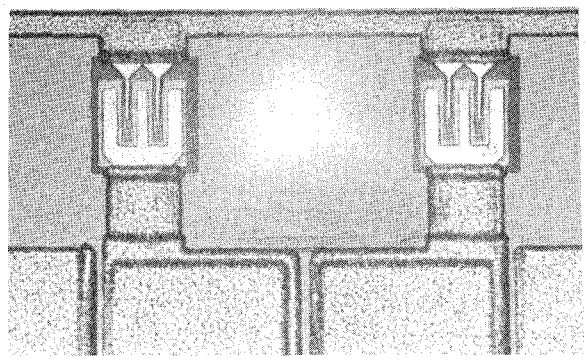

Figure 3 : Chip detail showing diodes.

D.C. breaks isolate the control signals from the r.f. input and output ports.

Owing to the lumped nature of the tapped lines their required electrical length is accommodated in half the distance that would otherwise have been necessary. This gives an efficient use of chip area and the complete 4-bit phase shifter chip occupies only 3.7 x 2.3 mm (146 x 90 mils).

After deciding the first prototype layout, parasitic inductances, capacitances and coupling effects were estimated by calculation and by constructing 100 times scale models for measurement at VHF. Design iterations enabled these parasitic effects to be accommodated.

FABRICATION

Active regions for the diodes and load resistors are selectively implanted into the SI substrate. The implant dose and anneal are chosen to give a peak concentration of 1.5 E18 at 0.4 μm depth and 1.5 E17 at the surface. Ohmic contact areas are etched down to the n^+ region prior to contact deposition and alloying in an optical furnace. Thus a low series resistance is achieved together with the required junction capacitance and breakdown voltage.

The remainder of the processing is fairly conventional: Si_3N_4 is used for passivation and for the capacitors; air bridges form the coupler cross-overs and give access to the capacitor top plates; all passive components are plated to a thickness of 5 μm.

MEASURED PERFORMANCE

At the time of writing the first chip has just been measured and demonstrates most of the expected features.

The linear phase/frequency characteristic is scarcely noticable over a 10% bandwidth as the measured results in Figure 4 demonstrate. Note that full 360° coverage is obtained with only 13 states; a consequence of a higher diode capacitance than assumed for the original design. Figure 5 shows similar measurements over all X-band.

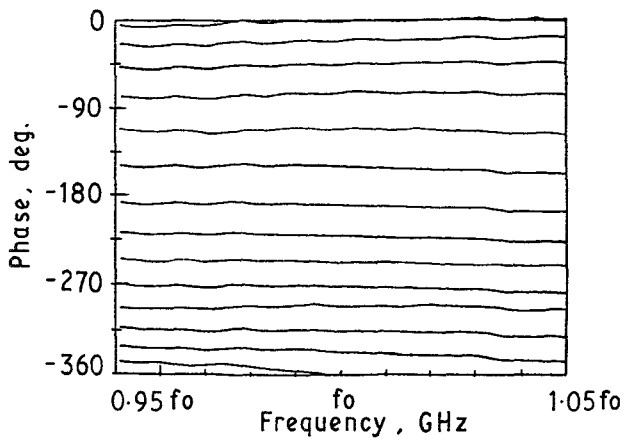

Figure 4 : Measured phase/frequency over 10% bandwidth.

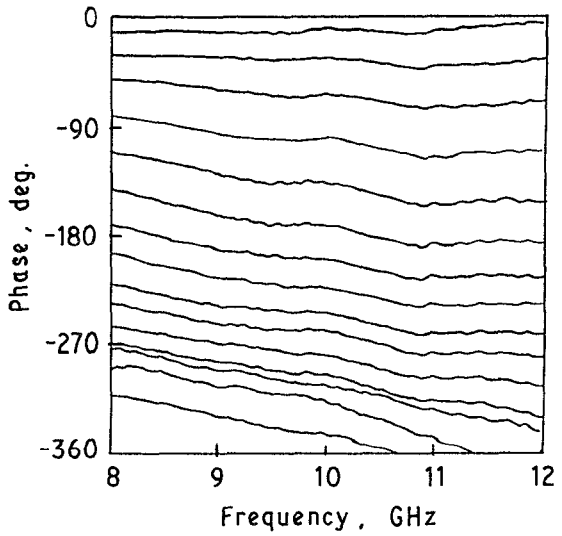

Figure 5 : Measured phase/frequency over X-band.

Input match is excellent; apart from a couple of isolated points it is better than 15 dB return loss for all phase states over the whole of X-band as illustrated for an arbitrary three states in Figure 6.

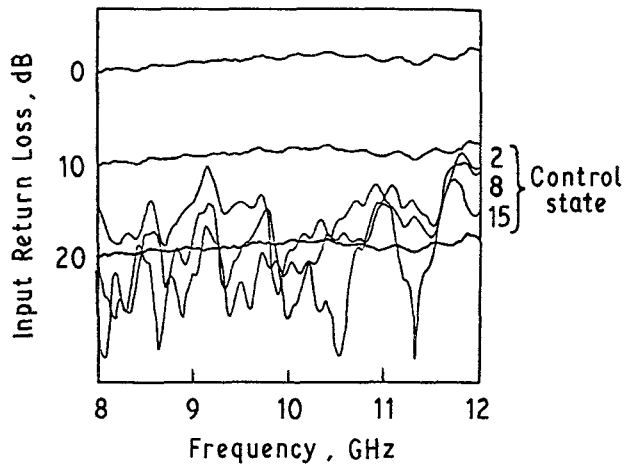

Figure 6 : Measured return loss over X-band for three arbitrary states.

Insertion loss lies between 5 dB and 8 dB for all states throughout X-band; three arbitrary states are illustrated in Figure 7.

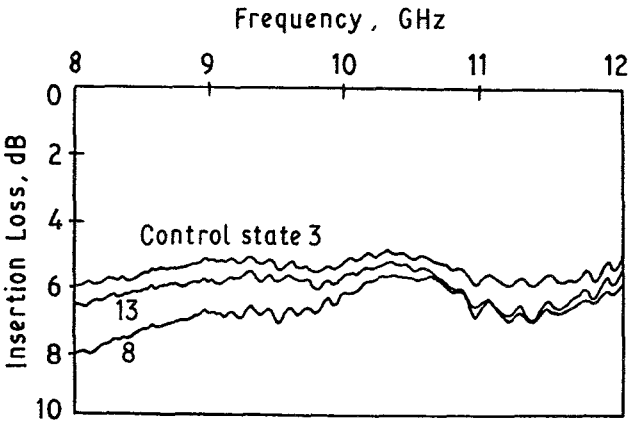

Figure 7 : Measured insertion loss over X-band for three arbitrary states.

Dynamic range is good; measurements at 20 mW (the highest available) were within 10° of the small signal values at all frequencies and phase states.

The same circuit has also been operated as a continuously variable phase shifter by setting the last pair of diodes to the on-state and varying the reverse bias simultaneously on all others. Continuous phase control over nearly 30° was achieved, Figure 8. Two identical chips, one with digital and one with analogue control could therefore be used for very precise phase setting.

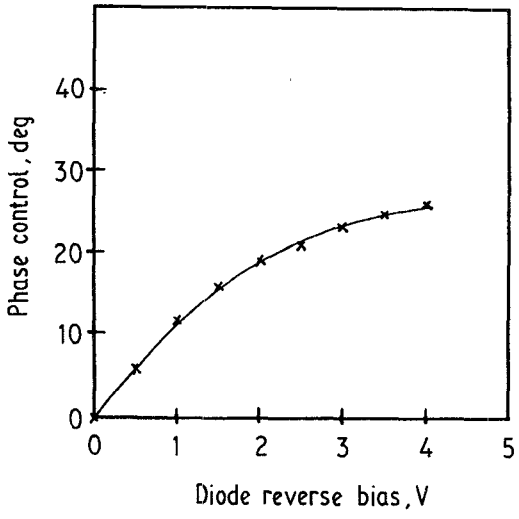

Figure 8 : Measured performance as continuously variable phase shifter.

The only features of the performance of this first chip which fall short of expectation are the linearity of the control characteristic (i.e. phase versus control state) and the average phase shift between successive control states which is 20% high. Diagnostic investigations have revealed a common, easily correctable, cause.

DIAGNOSIS

Measurements of test diodes provided on wafer revealed the diode junction (not stray) capacitance to be 40% high due to an excessive doping level at the surface. This accounts directly for the 20% high value of average phase shift between successive control states.

A second consequence of the high diode capacitance is a reduction in impedance of the artificial line resulting in a reflection from the junction of the line with the coupler. This can be represented by a state independent error vector which adds to the voltage vector representing the phase controlled signal. Where the error vector has a component in phase with the controlled vector the phase increment is reduced and where there is an anti-phase component the phase increment is enhanced. This is illustrated in the simplified vector diagram of Figure 9. It can also be seen from this figure that a variation in the amplitude of the resultant vector with control state should be expected.

A re-analysis of the circuit with the measured diode characteristics but with all other quantities as per the original design, accurately predicted both the high value of average phase shift between successive phase states and the non-linearity of the control characteristic as can be seen in Figure 10. An amplitude variation cycling between ±1 dB was also predicted in good agreement with the measurements (not illustrated).

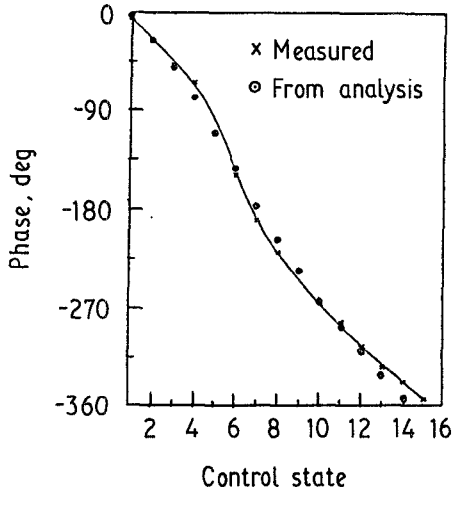

Figure 10: Measured and analysed control charateristic.

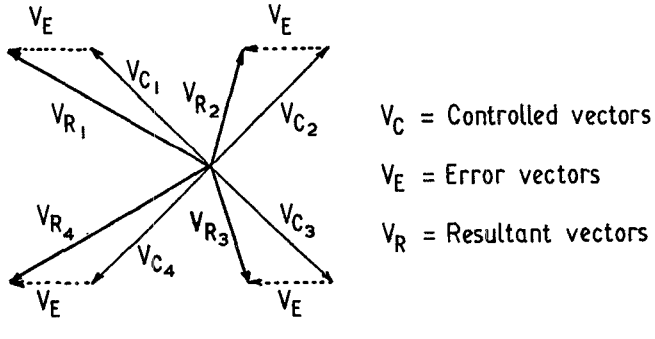

Figure 9 : Diagrammatic illustration of phase errors.

It has thus been established that these moderate non-idealities of the circuit are due to a gross 40% capacitance error. A high degree of correction is therefore confidently anticipated in future batches.

ACKNOLWEDGEMENT

The authors would like to thank their many colleagues whose contributions to this work were indispensable and in particular to Mr J W Burns who designed the test mounts and carried out the assessment.